Claims

We claim:

1. A switching regulator, comprising:

a driver coupled to receive a first high side reference voltage;

an input switching device having a source node, a drain node, and a control node, the control node coupled to an output of the driver, the drain node coupled to receive an input voltage;

a diode coupled between the source node of the input switching device and ground;

an inductor having a first end coupled to the source node of the input switching device;

a first output switching device having a drain node coupled to the second end of the inductor, the first output switching device having a control node coupled to a high side output;

a second output switching device having a drain node coupled to the second end of the inductor, the first output switching device having a control node coupled to a low side output;

an output load coupled to the source nodes of the first and second output switching devices; and

a low power control circuit coupled across the inductor, wherein the low power control circuit monitors the current across the output load and automatically initiates the low power mode of the switching regulator independent of the value of the output load and the input voltage.

2. A switching regulator as recited in claim 1, wherein the low power control circuit comprises:

a low power switching device having a control node coupled to the high side output and a drain node coupled to the second end of the inductor;

an amplifier coupled to the source node of the low power switching device and the first output switching device;

a first current mirror coupled to the amplifier to mirror the difference between the output current through the output load and the current supplied at the second end of the inductor;

a second current mirror coupled to the first current mirror;

a current source coupled to the second current mirror;

a capacitor coupled across the current source;

a comparator coupled to the second current mirror and coupled to receive a predetermined voltage source to compare the voltage across the capacitor with the predetermined voltage source;

a first AND gate coupled to the comparator and to receive the low power mode signal;

a second AND gate coupled to the comparator and to receive the low power mode signal and the inductive switch signal;

a first counter coupled to the first AND gate to provide a low power entry signal; and

a second counter coupled to the second AND gate to provide a low power exit signal.

3. The switching regulator as recited in claim 1, wherein the first input switching device is a transistor.

4. The switching regulator as recited in claim 1, wherein the second input switching device is a transistor.

5. The switching regulator as recited in claim 1, wherein the first output switching device is a transistor.

6. The switching regulator as recited in claim 1, wherein the second output switching device is a transistor.

7. The switching regulator as recited in claim 1, wherein the first input switching device is a metal-oxide-semiconductor field-effect transistor (Mos FET).

8. The switching regulator as recited in claim 1, wherein the second input switching device is a Mos FET transistor.

9. The switching regulator as recited in claim 1, wherein the first output switching device is a Mos FET transistor.

10. The switching regulator as recited in claim 1, wherein the second output switching device is a Mos FET transistor.

11. The switching regulator as recited in claim 1, wherein the output load comprises:

a capacitor; and

a resistor coupled in parallel with the capacitor.

12. The switching regulator as recited in claim 2, wherein the low power switching device is a transistor.

13. The switching regulator as recited in claim 2, wherein the low power switching device is a sense FET transistor.

14. The switching regulator as recited in claim 2, wherein the first current mirror, comprises:

a first transistor, having a drain node coupled to the source node of the low power switching device; and

a second transistor coupled to the first transistor, the control node of the first and second transistors couple to the amplifier, the source node of the second transistor coupled to the source node of the first transistor.

13. The switching regulator as recited in claim 2, wherein the second current mirror, comprises:

a first transistor, having a drain node, a source node, and a control node, the drain node coupled to the control node and the drain node coupled to the first current mirror; and

a second transistor having a drain node, a control node and a source node, the control node coupled to the control node of the first transistor, the source node coupled to the source node of the first transistor, the drain node coupled to the capacitor.